US009224839B2

(12) **United States Patent**
Akimoto et al.

(10) **Patent No.: US 9,224,839 B2**
(45) **Date of Patent: Dec. 29, 2015**

(54) **METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE**

(71) Applicant: **Semiconductor Energy Laboratory Co., Ltd.**, Atsugi-shi, Kanagawa-ken (JP)

(72) Inventors: **Kengo Akimoto**, Atsugi (JP); **Masashi Tsubuku**, Atsugi (JP)

(73) Assignee: **Semiconductor Energy Laboratory Co., Ltd.**, Kanagawa-ken (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **14/459,548**

(22) Filed: **Aug. 14, 2014**

(65) **Prior Publication Data**

US 2014/0357018 A1 Dec. 4, 2014

Related U.S. Application Data

(60) Continuation of application No. 13/207,449, filed on Aug. 11, 2011, now Pat. No. 8,809,115, which is a division of application No. 12/549,603, filed on Aug. 28, 2009, now Pat. No. 8,021,916.

(30) **Foreign Application Priority Data**

Sep. 1, 2008 (JP) 2008-224061

(51) **Int. Cl.**
H01L 21/16 (2006.01)
H01L 29/66 (2006.01)
(Continued)

(52) **U.S. Cl.**
CPC ***H01L 29/66742*** (2013.01); ***H01L 21/324*** (2013.01); ***H01L 21/447*** (2013.01); ***H01L 27/127*** (2013.01); ***H01L 27/1225*** (2013.01); ***H01L 29/7869*** (2013.01); *H01L 21/02554* (2013.01); *H01L 21/02565* (2013.01); *H01L 21/02631* (2013.01)

(58) **Field of Classification Search**
None
See application file for complete search history.

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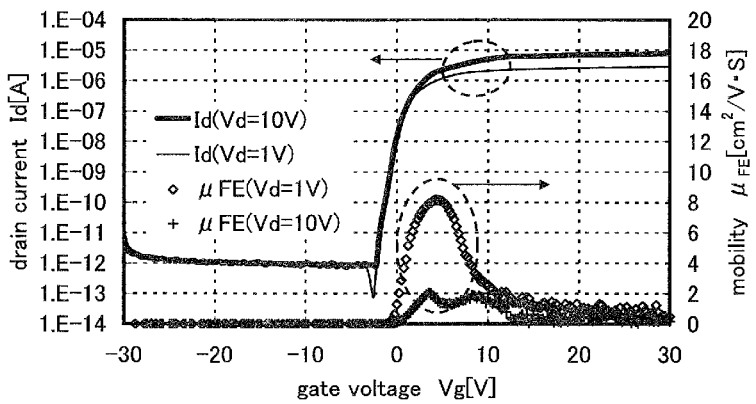
Primary Examiner — Yasser A Abdelaziez
(74) *Attorney, Agent, or Firm* — Robinson Intellectual Property Law Office; Eric J. Robinson

(57) **ABSTRACT**

To provide a method for manufacturing a thin film transistor in which contact resistance between an oxide semiconductor layer and source and drain electrode layers is small, the surfaces of the source and drain electrode layers are subjected to sputtering treatment with plasma and an oxide semiconductor layer containing In, Ga, and Zn is formed successively over the source and drain electrode layers without exposure of the source and drain electrode layers to air.

24 Claims, 7 Drawing Sheets



(51) **Int. Cl.**

H01L 27/12	(2006.01)
H01L 29/786	(2006.01)
H01L 21/324	(2006.01)
H01L 21/447	(2006.01)
H01L 21/02	(2006.01)

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Taiwanese Office Action (Application No. 100129731) Dated Mar. 20, 2014.

Korean Office Action (Application No. 2009-0081023) Dated Aug. 20, 2015.

FIG. 1A

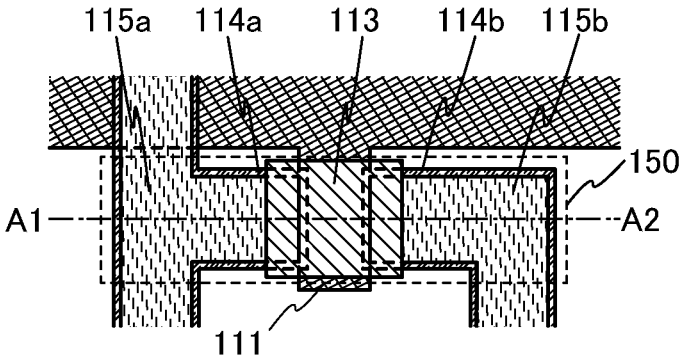

115a
114a
113
114b
115b
150
A1
A2
111

FIG. 1B

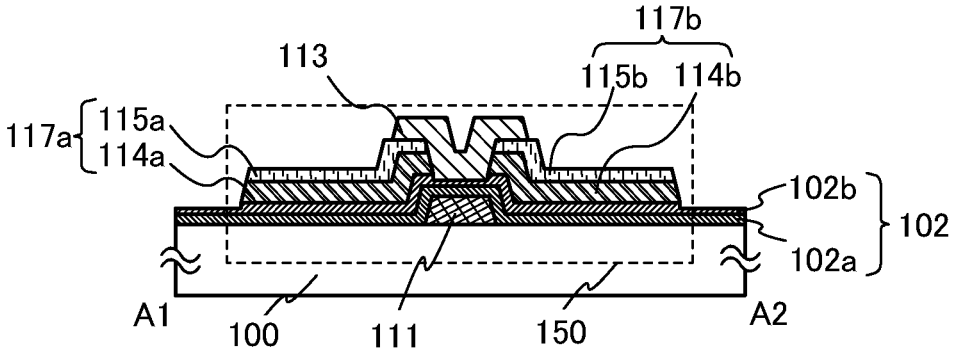

117b
113
115b
114b
117a
115a
114a
102b
102
102a
A1
A2
100
111
150

FIG. 2A

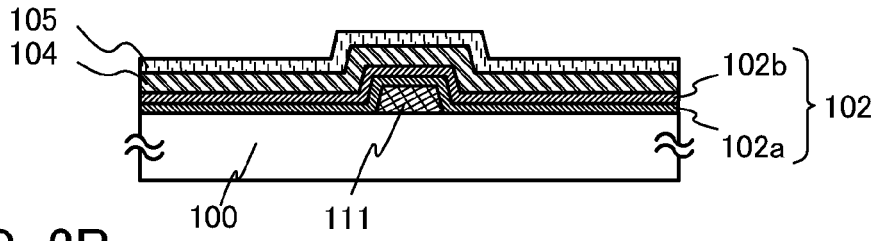


FIG. 2B

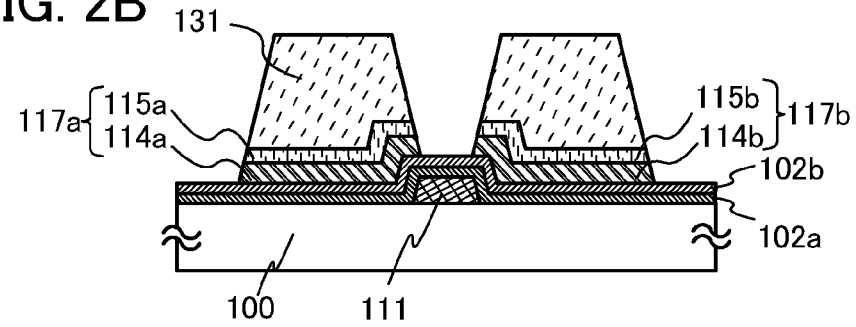


FIG. 2C

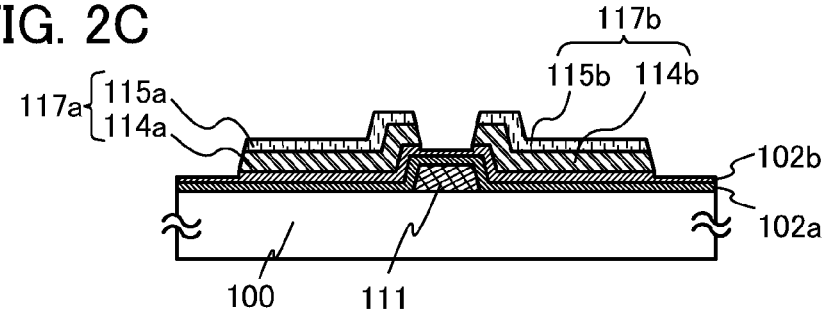


FIG. 2D

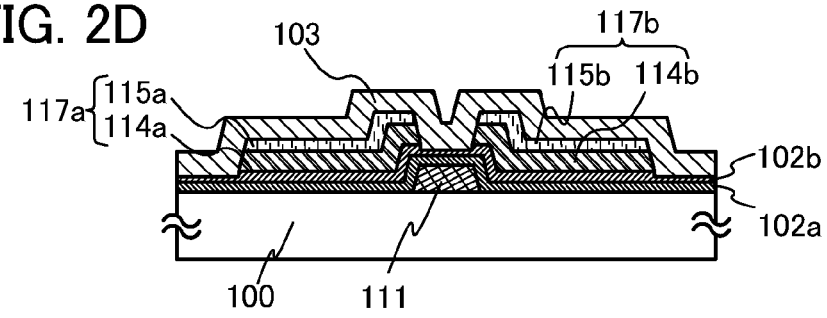


FIG. 2E

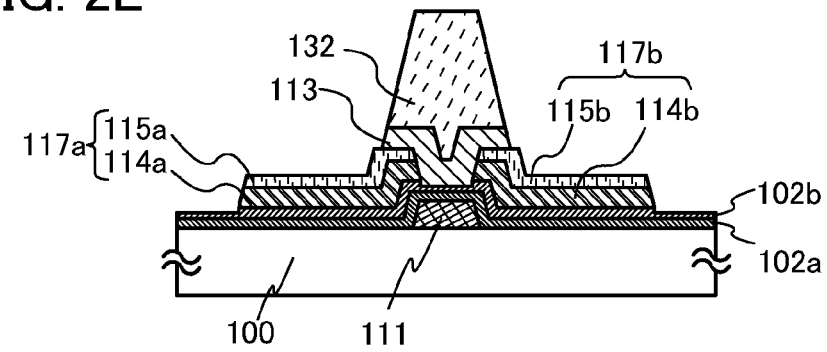


FIG. 3

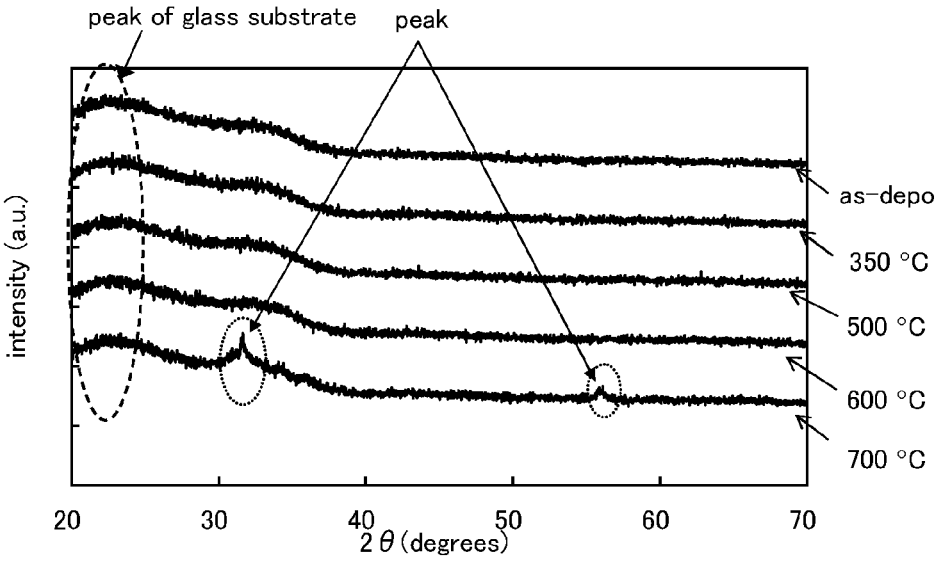

peak of glass substrate
peak
intensity (a.u.)
as-depo
350 °C
500 °C
600 °C
700 °C
20
30
40
50
60
70
2θ (degrees)

FIG. 4

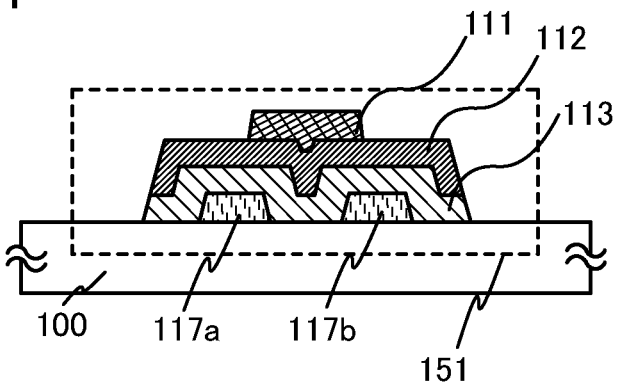


FIG. 5A

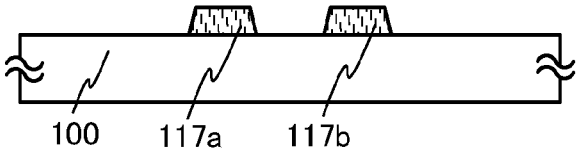


FIG. 5B

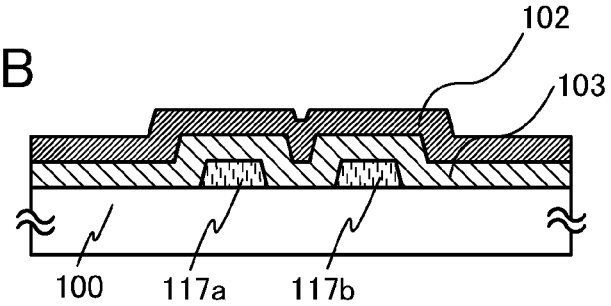


FIG. 5C

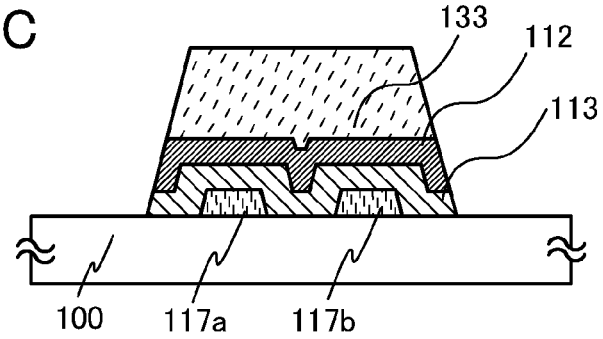


FIG. 5D

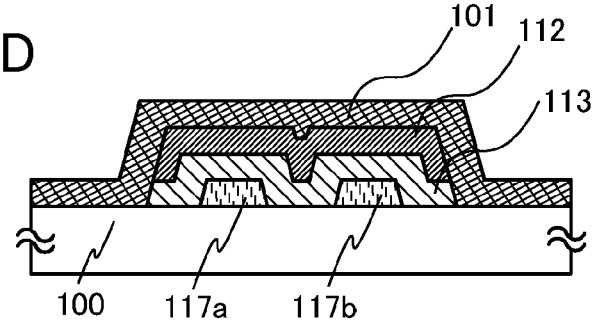


FIG. 5E

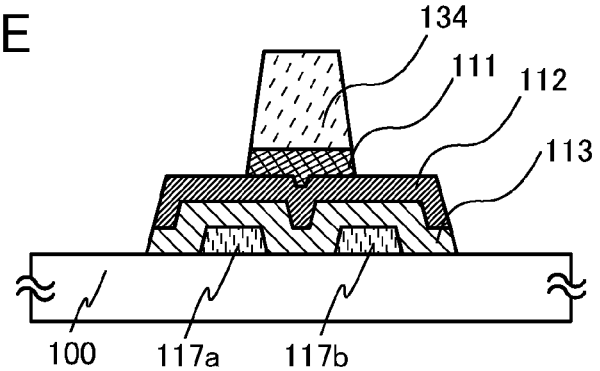


FIG. 6

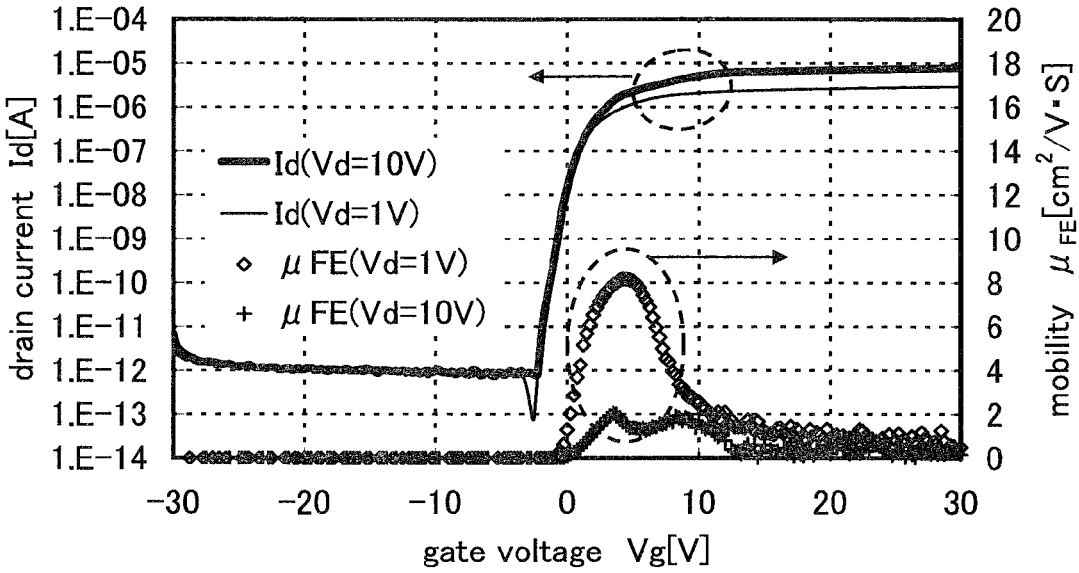
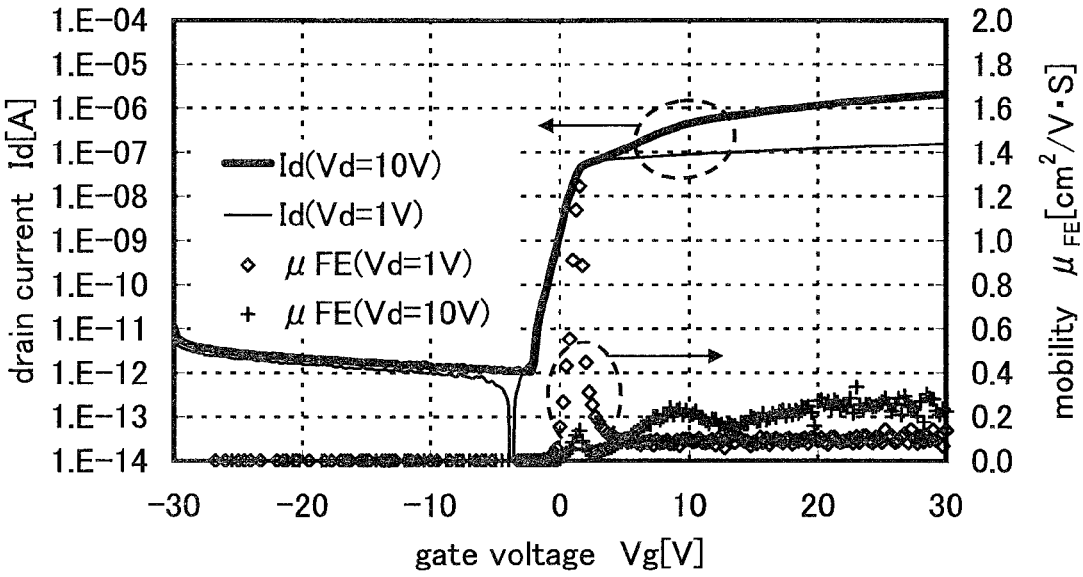

1.E-04
1.E-05
1.E-06
1.E-07
1.E-08
1.E-09
1.E-10
1.E-11
1.E-12
1.E-13
1.E-14
drain current Id[A]
Id(Vd=10V)
Id(Vd=1V)
μFE(Vd=1V)
μFE(Vd=10V)
20
18
16
14
12
10
8
6
4
2
0
mobility μFE[cm²/V·S]
-30
-20
-10
0
10
20
30
gate voltage Vg[V]

FIG. 7


1.E-04
1.E-05
1.E-06
1.E-07
1.E-08
1.E-09
1.E-10
1.E-11
1.E-12
1.E-13
1.E-14
drain current Id[A]
Id(Vd=10V)
Id(Vd=1V)
μFE(Vd=1V)
μFE(Vd=10V)
2.0
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
mobility μFE[cm²/V·S]
-30
-20
-10
0
10
20
30
gate voltage Vg[V]

METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method for manufacturing a semiconductor device which has a circuit including a thin film transistor (hereinafter, referred to as a TFT) in which a channel formation region is formed using an oxide semiconductor film. For example, the present invention relates to a method for manufacturing a semiconductor device which is mounted on an electro-optical device typified by a liquid crystal display panel or a light-emitting display device including an organic light-emitting element.

Note that the semiconductor device in this specification indicates all the devices which can operate by using semiconductor characteristics, and an electro-optical device, a semiconductor circuit, and an electronic appliance are all included in the semiconductor devices.

2. Description of the Related Art

In recent years, active-matrix display devices (such as liquid crystal display devices, light-emitting display devices, or electrophoretic display devices) in which a switching element of a thin film transistor (TFT) is provided for each of display pixels arranged in matrix have been actively developed. In the active-matrix display devices, a switching element is provided for each of pixels (or each of dots), and thus, there is such an advantage that the active matrix display devices can be driven at lower voltage than passive matrix display devices in the case where the pixel density is increased.

In addition, a technique has attracted attention, where a thin film transistor (TFT) or the like in which a channel formation region is formed using an oxide semiconductor film is applied to electronic devices or optical devices. For example, a TFT in which ZnO is used for an oxide semiconductor film or a TFT in which $InGaO_3(ZnO)_m$ is used for an oxide semiconductor film can be given. A technique in which a TFT including such an oxide semiconductor film is formed over a light-transmitting substrate and used as a switching element or the like of an image display device is disclosed in Patent Document 1 and Patent Document 2.

REFERENCES

Patent Document

[Patent Document 1] Japanese Published Patent Application No. 2007-123861

[Patent Document 2] Japanese Published Patent Application No. 2007-96055

SUMMARY OF THE INVENTION

In forming a thin film transistor, source and drain electrode layers are formed using a low resistance metal material. In particular, in the case of manufacturing display devices performing large-area display, the problem of signal delay due to wiring resistance becomes significant. Therefore, a metal material having low electric resistance is preferably used as a material of a wiring or an electrode.

Further, when contact resistance between the source and drain electrode layers and the oxide semiconductor film is high, ON current is suppressed. One of the causes which make the contact resistance high is that an interface at which the source and drain electrode layers and the oxide semiconductor film are in contact with each other has high electrical resistance due to a film of oxide or contaminant generated on the surfaces of the source and drain electrode layers.

An object of the present invention is to provide a method for manufacturing a thin film transistor in which contact resistance between an oxide semiconductor layer containing indium(In), gallium(Ga), and zinc(Zn) and source and drain electrode layers is small.

The gist of the present invention includes a method for manufacturing a semiconductor device in which after sputtering treatment with plasma is performed on surfaces of source and drain electrode layers, an oxide semiconductor layer containing In, Ga, and Zn is successively formed over the source and drain electrode layers without exposure of the surfaces of the source and drain electrode layers to air.

In this specification, a semiconductor layer formed using an oxide semiconductor film containing In, Ga, and Zn is also referred to as an "IGZO semiconductor layer".

The source and drain electrode layers are formed through a patterning step by a photolithography method, an ink-jet method, or the like. However, a film of oxide or contaminant is formed on the surfaces of the source and drain electrode layers in the patterning step unintentionally in some cases. When the oxide semiconductor layer containing In, Ga, and Zn is formed over the film of oxide or contaminant, contact resistance between the oxide semiconductor layer and the source and drain electrode layers is increased.

In the present invention, a film of oxide or contaminant on the surfaces of the source and drain electrode layers is removed by sputtering treatment with plasma, and further, an oxide semiconductor layer containing In, Ga, and Zn is formed successively with the surfaces of the source and drain electrode layers kept clean and not exposed to air.

One embodiment of the present invention is a method for manufacturing a semiconductor device including steps of performing sputtering treatment with plasma on surfaces of source and drain electrode layers and forming an oxide semiconductor layer containing In, Ga, and Zn successively over the source and drain electrode layers without exposure of the source and drain electrode layers to air.

Another embodiment of the present invention is a method for manufacturing a semiconductor device including steps of forming a gate electrode layer over a substrate; forming a gate insulating film which covers the gate electrode layer; forming source and drain electrode layers end portions of which overlap with the gate electrode layer with the gate insulating film interposed therebetween; performing sputtering treatment with plasma on surfaces of the source and drain electrode layers; and forming an oxide semiconductor layer containing indium, gallium, and zinc over the source and drain electrode layers without exposure of the source and drain electrode layers to air.

Another embodiment of the present invention is a method for manufacturing a semiconductor device including steps of forming source and drain electrode layers over a substrate; performing sputtering treatment with plasma on surfaces of the source and drain electrode layers; forming an oxide semiconductor layer containing indium, gallium, and zinc successively over the source and drain electrode layers without exposure of the surfaces of the source and drain electrode layers to air; forming a gate insulating film which covers the oxide semiconductor layer; and forming a gate electrode layer over a channel formation region of the oxide semiconductor layer with the gate insulating film interposed therebetween.

Another embodiment of the present invention is the method for manufacturing a semiconductor device in which

the plasma treatment is performed on the surfaces of the source and drain electrode layers in an inert gas atmosphere.

By applying one embodiment of the present invention, the surfaces of the source and drain electrode layers are cleaned and the oxide semiconductor layer containing In, Ga, and Zn can be formed over the source and drain electrode layers with the surfaces of the source and drain electrode layers kept clean; therefore, contact resistance between the source and drain electrode layers and the oxide semiconductor layer containing In, Ga, and Zn can be reduced. As a result, a thin film transistor having a high on/off ratio can be manufactured. Further, a method for manufacturing a semiconductor device having favorable electrical properties and reliability with high productivity can be provided.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings:

FIGS. **1**A and **1**B are views illustrating a structure of a thin film transistor which is manufactured in the present invention;

FIGS. **2**A to **2**E are views illustrating a method for manufacturing a thin film transistor of the present invention;

FIG. **3** is an X-ray diffraction pattern of an oxide semiconductor layer containing In, Ga, and Zn which is used in the present invention;

FIG. **4** is a view illustrating a structure of a thin film transistor which is manufactured in the present invention;

FIGS. **5**A to **5**E are views illustrating a method for manufacturing a thin film transistor of the present invention;

FIG. **6** is a chart showing electrical properties of a thin film transistor to which the present invention is applied; and

FIG. **7** is a chart showing electrical properties of a thin film transistor which is manufactured as a comparative example.

DETAILED DESCRIPTION OF THE INVENTION

Hereinafter, embodiments and an example of the present invention will be described with reference to the accompanying drawings. Note that it is easily understood by those skilled in the art that the present invention is not limited to the description below and that a variety of changes can be made in forms and details without departing from the spirit and the scope of the present invention. Therefore, the present invention is not to be construed with limitation to what is described in the embodiments and the example. Note that in a structure of the present invention described below, like portions or portions having like functions in different drawings are denoted by the like reference numerals and repeated description thereof is omitted.

[Embodiment 1]

In this embodiment, a thin film transistor and a manufacturing process thereof will be described with reference to FIGS. **1**A and **1**B and FIGS. **2**A to **2**E.

FIGS. **1**A and **1**B illustrate a bottom gate thin film transistor of this embodiment. FIG. **1**A is a plan view and FIG. **1**B is a cross-sectional view taken along line A**1**-A**2** in FIG. **1**A. In a thin film transistor **150** illustrated in FIGS. **1**A and **1**B, a gate electrode layer **111** is formed over a substrate **100**, a gate insulating film **102** is formed over the gate electrode layer **111**, source and drain electrode layers **117***a* and **117***b* are formed over the gate electrode layer **111** with the gate insulating film **102** interposed therebetween, and a semiconductor layer **113** which serves as a channel formation region is formed between the source and drain electrode layers **117***a* and **117***b*. Note that in this embodiment, the gate insulating film **102** includes two layers, a first gate insulating film **102***a* and a second gate insulating film **102***b*.

In FIG. **1**B, the source and drain electrode layers (**117***a* and **117***b*) include a layer containing aluminum as its main component (**114***a* and **114***b*) and a high-melting-point metal material layer (**115***a* and **115***b*), respectively. Sputtering treatment with plasma is performed on surfaces of the source and drain electrode layers (**117***a* and **117***b*) and a region of a surface of the second gate insulating film (**102***b*) which is not covered with the source and drain electrode layers (**117***a* and **117***b*), so that a film of oxide or contaminant is removed.

In the present invention, an oxide semiconductor containing In, Ga, and Zn is used as the semiconductor layer **113**. An oxide semiconductor layer containing In, Ga, and Zn absorb little light and is not photoexcited easily; therefore, it is not necessary to shield the channel formation region from light by covering the channel formation region with the gate electrode layer.

A method for manufacturing the thin film transistor **150** illustrated in FIGS. **1**A and **1**B will be described with reference to FIGS. **2**A to **2**E.

As the substrate **100**, any of the following substrates can be used: non-alkaline glass substrates manufactured by a fusion method or a float method, such as a barium borosilicate glass substrate, an aluminoborosilicate glass substrate, an aluminosilicate glass substrate, and the like; ceramic substrates; plastic substrates having heat resistance high enough to withstand a process temperature of this manufacturing process; and the like. Alternatively, a metal substrate of a stainless alloy or the like, which is provided with an insulating film over its surface, may be used. In the case where the substrate **100** is mother glass, the substrate may have any of the following sizes: the first generation (320 mm×400 mm), the second generation (400 mm×500 mm), the third generation (550 mm×650 mm), the fourth generation (680 mm×880 mm or 730 mm×920 mm), the fifth generation (1000 mm×1200 mm or 1100 mm×1250 mm), the sixth generation (1500 mm×1800 mm), the seventh generation (1900 mm×2200 mm), the eighth generation (2160 mm×2460 mm), the ninth generation (2400 mm×2800 mm or 2450 mm×3050 mm), the tenth generation (2950 mm×3400 mm), and the like.

Further, an insulating film may be provided as a base film over the substrate **100**. The base film can be formed to have a single-layer structure or a stacked structure of a silicon oxide film, a silicon nitride film, a silicon oxynitride film, and/or a silicon nitride oxide film by a CVD method, a sputtering method, or the like.

The gate electrode layer **111** is formed using a metal material. As the metal material, aluminum, chromium, titanium, tantalum, molybdenum, copper, or the like is applied. The gate electrode layer may be a single conductive film and as a preferable example, the gate electrode layer is formed using a layer containing aluminum as its main component or has a stacked layer structure in which a layer containing aluminum as its main component and a barrier metal layer are stacked.

For a layer containing aluminum as its main component, an aluminum alloy to which an element which improves heat resistance or an element which prevents hillock, such as tungsten, titanium, tantalum, molybdenum, nickel, platinum, copper, gold, silver, manganese, carbon, or silicon, or an alloy material or a compound which contains any of these elements as its main component is added is used.

As a barrier metal layer, a high-melting-point metal, such as titanium, molybdenum, or chromium, is used. The barrier metal layer is preferably provided so as to prevent hillock or oxidation of aluminum.

A conductive film which is to be the gate electrode layer **111** is formed to a thickness greater than or equal to 50 nm and less than or equal to 300 nm. By forming the gate electrode layer **111** to a thickness less than or equal to 300 nm, disconnection of a semiconductor film and wirings which are to be formed later can be prevented. Further, by forming the gate electrode layer **111** to a thickness greater than or equal to 150 nm and less than or equal to 300 nm, resistance of the gate electrode layer can be reduced and thus the size of the substrate can be increased.

Note that since a semiconductor film is to be formed over the gate electrode layer **111**, it is desired that the gate electrode layer **111** be processed to have tapered end portions in order to prevent disconnection. In addition, although not illustrated, in this step, a wiring or a capacitor wiring connected to the gate electrode layer can also be formed at the same time.

The gate electrode layer **111** can be formed by a sputtering method, a CVD method, a plating method, a printing method, or the like. Alternatively, the gate electrode layer **111** can be formed by discharging a conductive nanopaste of silver, gold, copper, or the like by an ink-jet method and baking it.

Note that here, an aluminum film and a molybdenum film are deposited so as to be stacked by a sputtering method as a conductive film over the substrate. Next, with the use of a resist mask formed using a first photomask in this embodiment, the conductive film is etched to form the gate electrode layer **111**.

The gate insulating films **102***a* and **102***b* can each be formed using a silicon oxide film, a silicon nitride film, a silicon oxynitride film, or a silicon nitride oxide film with a thickness of from 50 nm to 150 nm. Note that instead of a two-layer structure, the gate insulating film can be formed as a single layer of a silicon oxide film, a silicon nitride film, a silicon oxynitride film, or a silicon nitride oxide film. Alternatively, the gate insulating film may be formed to have a three-layer structure.

The gate insulating film **102***a* is formed using a silicon nitride film or a silicon nitride oxide film, whereby adhesion between the substrate and the first gate insulating film **102***a* is increased. In the case where a glass substrate is used as the substrate, an impurity can be prevented from diffusing into the semiconductor layer **113** from the substrate and further, the gate electrode layer **111** can be prevented from being oxidized. That is to say, film peeling can be prevented, and thus electrical properties of a thin film transistor which is completed later can be improved. Further, the first gate insulating film **102***a* and the second gate insulating film **102***b* each preferably have a thickness greater than or equal to 50 nm so that they can cover unevenness of the gate electrode layer **111**.

Here, a silicon oxynitride film means a film that contains more oxygen than nitrogen and includes oxygen, nitrogen, silicon, and hydrogen at concentrations ranging from 55 at. % to 65 at. %, 1 at. % to 20 at. %, 25 at. % to 35 at. %, and 0.1 at. % to 10 at. %, respectively. Further, a silicon nitride oxide film means a film that contains more nitrogen than oxygen and includes oxygen, nitrogen, silicon, and hydrogen at concentrations ranging from 15 at. % to 30 at. %, 20 at. % to 35 at. %, 25 at. % to 35 at. %, and 15 at. % to 25 at. %, respectively.

Further, for the gate insulating film **102***b* in contact with the semiconductor layer **113**, silicon oxide, aluminum oxide, magnesium oxide, aluminum nitride, yttrium oxide, or hafnium oxide can be used for example.

The first gate insulating film **102***a* and the second gate insulating film **102***b* can each be formed by a CVD method, a sputtering method, or the like. Here, as illustrated in FIG. **2**A, a silicon nitride film is formed by a plasma CVD method as the first gate insulating film **102***a* and a silicon oxide film is formed by a plasma CVD method as the second gate insulating film **102***b*.

In this embodiment, conductive films which are to be the source and drain electrode layers include a first conductive film **104** and a second conductive film **105**. The first conductive film **104** and the second conductive film **105** can be formed by a sputtering method or a vacuum evaporation method.

The conductive films which are to be source and drain electrode layers can be formed using the same material as the gate electrode layer **111**. Here, as illustrated in FIG. **2**A, the conductive film **104** containing aluminum as its main component and the conductive film **105** formed using a high-melting-point metal material are stacked.

For the conductive film **105** formed using a high-melting-point metal material, titanium, tantalum, tungsten, molybdenum, or the like can be used. In particular, it is preferable that a titanium film be a layer in contact with the oxide semiconductor layer containing In, Ga, and Zn. As a specific example of the conductive film, a single titanium film, a stacked film of a titanium film and an aluminum film, or a three-layer structure in which a titanium film, an aluminum film, and a titanium film are stacked in this order may be used.

Further, as the conductive film **105**, a transparent conductive film may be used, and as a material thereof, indium tin oxide, indium tin oxide containing silicon or silicon oxide, indium zinc oxide, zinc oxide, or the like can be used.

Next, a resist mask **131** is formed over the conductive films **104** and **105** by a photolithography method or an ink-jet method. With the use of the resist mask **131**, the conductive films **104** and **105** over the gate insulating film **102***b* are selectively etched to form the source and drain electrode layers (**117***a* and **117***b*) as illustrated in FIG. **2**B.

Note that since a semiconductor film is to be formed over the source and drain electrode layers (**117***a* and **117***b*), it is desired that the source and drain electrode layers be processed so as to have tapered end portions in order to prevent disconnection.

Not only an atmospheric component but also a variety of substances are in contact with surfaces of the source and drain electrode layers (**117***a* and **117***b*) in a patterning step. For example, in the case of using a photolithography technique, a resist or a remover of the resist are in contact with the surfaces of the source and drain electrode layers. Alternatively, in the case of using an ink-jet method, an additive such as a solvent or a dispersant contained in the ink are in contact with the surfaces of the source and drain electrode layers. As a result, a film of oxide or contaminant is formed on the surfaces of the source and drain electrode layers (**117***a* and **117***b*). The film of oxide or contaminant causes increase in contact resistance with the oxide semiconductor layer containing In, Ga, and Zn.

Next, in order to remove the film of oxide or contaminant which is formed on the surfaces of the source and drain electrode layers (**117***a* and **117***b*), sputtering treatment with plasma is performed on the surfaces of the source and drain electrode layers (**117***a* and **117***b*), so that the surfaces of the conductive films are cleaned. As a gas used in the sputtering, an inert gas with respect to the source and drain electrode layers is used. For example, a rare gas such as Ar can be given as an example thereof. Note that oxygen or the like may be mixed with the gas as long as a film of oxide or the like which increases contact resistance is not formed on the surfaces of the source and drain electrode layers.

As a method of sputtering treatment with plasma, a reverse sputtering method can be employed, for example. A reverse

sputtering method is a method in which without application of voltage to a target side in a sputtering apparatus, voltage is applied to a substrate side under an inert gas (e.g. an argon gas) atmosphere and plasma is generated on the substrate side to etch the surface of the substrate.

The conditions of a reverse sputtering method are as follows: RF sputtering is performed with a pressure in a chamber of preferably 0.2 Pa to 4.0 Pa using an Ar gas with a power of preferably 50 W to 2 kW.

As a result of the sputtering treatment with plasma, the surfaces of the source and drain electrode layers (**117***a* and **117***b*) are cleaned.

Note that as illustrated in FIG. **2**C, a region of the surface of the gate insulating film (**102***b*) which is not covered with the source and drain electrode layers (**117***a* and **117***b*) and the surfaces of the source and drain electrode layers (**117***a* and **117***b*) are subjected to sputtering treatment with plasma, and therefore, are slightly reduced in thickness in some cases.

Next, without exposure of the surfaces of the source and drain electrode layers (**117***a* and **117***b*) on which sputtering treatment with plasma has been performed to air, deposition of the semiconductor film **103** over the source and drain electrode layers (**117***a* and **117***b*) is performed as illustrated in FIG. **2**D, following the plasma treatment. The semiconductor film **103** is deposited successively without exposure of the surfaces on which the sputtering treatment with plasma has been performed to air, whereby an atmospheric component or contaminant in air can be prevented from attaching to the surfaces, so that the surfaces can be kept clean.

As a method for depositing the semiconductor film **103** successively without exposure of the surfaces of the source and drain electrode layers (**117***a* and **117***b*) on which the sputtering treatment with plasma has been performed to air, a method of using a multichamber manufacturing apparatus in which a plasma treatment chamber and a deposition chamber of the semiconductor film **103** are connected to each other can be given as an example.

Further, in the case of depositing an oxide semiconductor film **103** containing In, Ga, and Zn by a sputtering method, the method in which a reverse sputtering method is performed on the surfaces of the source and drain electrode layers in a deposition chamber of the semiconductor film **103** before formation of the semiconductor film **103** is preferable since the apparatus and the step of the method are simple.

As the semiconductor film **103**, an oxide containing In, Ga, and Zn can be used. In the case of using an oxide containing In, Ga, and Zn as the semiconductor film **103**, the oxide containing In, Ga, and Zn is formed to a thickness greater than or equal to 2 nm and less than or equal to 200 nm, preferably greater than or equal to 20 nm and less than or equal to 150 nm. Further, when the oxygen vacancy rate in the film is increased, a carrier concentration is increased and thus thin film transistor characteristics are degraded. Therefore, the oxide containing In, Ga, and Zn is deposited in an atmosphere containing oxygen.

An oxide semiconductor containing In, Ga, and Zn can be deposited by a reactive sputtering method or a pulsed laser deposition method (PLD method). Among vapor deposition methods, a PLD method is suitable in terms of ease of controlling a composition of materials, and a sputtering method is suitable in terms of mass productivity.

Here, a target with a diameter of 8 inch obtained by mixing indium oxide (In_2O_3), gallium oxide (Ga_2O_3), and zinc oxide (ZnO) in an equimolar ratio and performing sintering is used, a substrate is provided 170 mm apart from the target, and direct current (DC) sputtering is performed with a power of 500 W, so that the semiconductor film is formed. The semiconductor film is formed to a thickness of 50 nm under the conditions that the chamber pressure is 0.4 Pa and the gas composition ratio of Ar to O_2 is 10 to 5 sccm. It is desirable that an oxygen partial pressure in film formation be set higher than that in forming a transparent conductive film of indium tin oxide (ITO) or the like to control the oxygen concentration in a film formation atmosphere so that oxygen vacancy is suppressed. Further, it is preferable to use a pulsed direct current (DC) power supply because dusts can be reduced and the thickness distribution of the semiconductor film can be uniform.

Next, a resist mask **132** is formed over the semiconductor film **103** by a photolithography technique or an ink-jet method. With the use of the resist mask **132**, the semiconductor film **103** is selectively etched by dry etching or wet etching to form the semiconductor layer **113** as illustrated in FIG. **2**E.

As an example of a method for etching the oxide semiconductor film containing In, Ga, and Zn, an organic acid such as a citric acid or an oxalic acid can be used as an etchant. For example, the semiconductor film **103** with a thickness of 50 nm can be processed by etching with ITO07N (manufactured by Kanto Chemical Co., Inc.) in 150 seconds.

In a thin film transistor using the oxide semiconductor containing In, Ga, and Zn, the oxide semiconductor layer **113** is subjected to heat treatment, whereby the characteristics thereof are improved.

Since high energy is provided to a target with an Ar ion in a sputtering method, in the case of depositing an IGZO film by a sputtering method, it is considered that high strain energy exists in the IGZO film which is deposited and the strain energy inhibits carrier transfer. In order to release this strain energy, heat treatment is performed at 200° C. to 600° C., typically 300° C. to 500° C. It is considered that rearrangement at an atomic level is performed by this heat treatment, and thus the strain energy which inhibits carrier transfer is released. From such a reason, heat treatment after the deposition (including light annealing) is important.

Change of the oxide semiconductor film containing In, Ga, and Zn with heat treatment was investigated by an X-ray diffraction (XRD) method. As a sample, an IGZO film with a thickness of 400 nm was deposited over a glass substrate by a DC sputtering method. FIG. **3** is an XRD chart.

First, the XRD chart of the IGZO film right after the deposition is denoted by "as-depo" in FIG. **3**. XRD charts of the samples on which heat treatment was performed at different temperatures for one hour in a nitrogen atmosphere after the deposition are illustrated in FIG. **3** together with the process temperatures. That is, FIG. **3** shows charts of the samples on which heat treatment was performed at 350° C., 500° C., 600° C., and 700° C. Note that in order to compare the charts of the different samples, the charts are arranged for convenience.

In the sample on which the heat treatment was performed at 700° C., peaks indicating crystallization were observed clearly in the ranges of $30° \leq 2\theta \leq 35°$ and $55° \leq 2\theta \leq 60°$. Further, when the heat treatment is performed at higher than or equal to 700° C., clear crystallization is observed.

However, when the heat treatment is performed at 200° C. to 600° C., crystal growth due to great transfer of atoms does not occur unlike when the heat treatment is performed at higher than or equal to 700° C.

In this embodiment, the heat treatment is performed on the oxide semiconductor film **103** containing In, Ga, and Zn at 350° C. for one hour. The heat treatment may be performed in any step after deposition of the semiconductor film **103**. For example, the heat treatment may be performed after deposition of the semiconductor film **103** or after formation of the semiconductor layer **113**. Alternatively, the heat treatment

may be performed after formation of a sealing film of a thin film transistor or may be performed by another heat treatment such as thermal cure treatment which is performed after formation of a planarization film.

Further, plasma treatment may be performed on the semiconductor layer **113**. By the plasma treatment, damage due to the etching which is performed in forming the semiconductor layer **113** can be repaired. The plasma treatment is preferably performed in an atmosphere containing O_2, N_2O, preferably oxygen. Note that as a specific example of an atmosphere containing oxygen, a gas in which oxygen is added to N_2, He, Ar, or the like can be given. Alternatively, the plasma treatment may be performed in an atmosphere in which Cl_2 and CF_4 are added to the above atmosphere. Note that the plasma treatment is preferably performed with non-bias applied.

By the method described above, the bottom gate thin film transistor illustrated in FIGS. **1**A and **1**B is manufactured.

According to this embodiment, with the surfaces of the source and drain electrode layers kept clean, the oxide semiconductor layer containing In, Ga, and Zn can be formed; therefore, a thin film transistor in which contact resistance between the source and drain electrode layers and the oxide semiconductor layer containing In, Ga, and Zn is reduced can be provided.

Accordingly, by applying the present invention, a thin film transistor having a high on/off ratio can be manufactured. Further, a semiconductor device which includes a thin film transistor having favorable electrical characteristics and reliability can be provided by a method which is excellent in productivity.

(Embodiment 2)

In this embodiment, a thin film transistor mode of which is different from that in Embodiment 1 and a manufacturing process of the thin film transistor will be described with reference to FIG. **4** and FIGS. **5**A to **5**E. FIG. **4** is a cross-sectional view illustrating a staggered thin film transistor of this embodiment. In a thin film transistor **151** illustrated in FIG. **4**, the source and drain electrode layers (**117***a* and **117***b*) are formed over the substrate **100** and the semiconductor layer **113** is formed so as to cover the source and drain electrode layers (**117***a* and **117***b*). A gate insulating layer **112** is formed over the semiconductor layer **113** and the gate electrode layer **111** is formed so as to overlap with the channel formation region with the gate insulating layer **112** interposed therebetween.

In FIG. **4**, the source and drain electrode layers (**117***a* and **117***b*) are formed using a high-melting-point metal material layer. Sputtering treatment with plasma is performed on the surfaces of the source and drain electrode layers (**117***a* and **117***b*), and thus a film of oxide or contaminant is removed.

In the present invention, an oxide semiconductor containing In, Ga, and Zn is used as the semiconductor layer **113**. An oxide semiconductor layer containing In, Ga, and Zn absorb little light and is not photoexcited easily; therefore, it is not necessary to shield the channel formation region from light by covering the channel formation region with the gate electrode layer. In other words, in the channel formation region, an overlap with the gate electrode layer and the source and drain electrode layers can be reduced, so that parasitic capacitance can be reduced.

A method for manufacturing the thin film transistor **151** illustrated in FIG. **4** will be described with reference to FIGS. **5**A to **5**E.

As the substrate **100**, a substrate similar to that in Embodiment 1 can be used. In this embodiment, a non-alkali glass substrate is used.

As a conductive film which is to be the source and drain electrode layers, the same material as that of the gate electrode layer **111** which is described in Embodiment 1 can be used. The conductive film which is to be the source and drain electrode layers can be deposited by a sputtering method or a vacuum evaporation method.

The conductive film which is to be the source and drain electrode layers may be a single layer or a plurality of layers. In particular, a layer in contact with the oxide semiconductor layer containing In, Ga, and Zn is preferably a titanium film.

In this embodiment, the pair of source and drain electrode layers (**117***a* and **117***b*) is formed using a high-melting-point metal material as illustrated in FIG. **5**A. Such minute processing can be performed using a resist mask formed by a photolithography technique or an ink-jet method.

Note that since a semiconductor film is to be formed over the source and drain electrode layers (**117***a* and **117***b*), it is desired that the source and drain electrode layers be processed so as to have tapered end portions in order to prevent disconnection.

Not only an atmospheric component but also a variety of substances are in contact with surfaces of the source and drain electrode layers (**117***a* and **117***b*) in the patterning step, and thus a film of oxide or contaminant is formed on the surfaces of the source and drain electrode layers (**117***a* and **117***b*).

Here, the film of oxide or contaminant on the surfaces of the source and drain electrode layers (**117***a* and **117***b*) is removed by a reverse sputtering method. As in Embodiment 1, a reverse sputtering method can be performed with the use of a sputtering apparatus in which the oxide semiconductor layer containing In, Ga, and Zn is formed.

As a gas used in the sputtering, an inert gas with respect to the source and drain electrode layers is used. Here, RF sputtering is performed under the following conditions: Ar is used as a gas used in the sputtering, the pressure in a chamber is preferably 0.2 Pa to 4.0 Pa, and a power is preferably 50 W to 2 kW.

Note that when sputtering treatment with plasma is performed on the substrate surface or in the case where the base film is formed on the substrate surface, a portion of a base film which is not covered with the source and drain electrode layers (**117***a* and **117***b*), slight reduction in thickness is caused in some cases.

Next, without exposure of the surfaces of the source and drain electrode layers (**117***a* and **117***b*) on which sputtering treatment with plasma has been performed to air, deposition of the oxide semiconductor film **103** over the source and drain electrode layers (**117***a* and **117***b*) is performed following the plasma treatment. Note that the deposition conditions of the oxide semiconductor film containing In, Ga, and Zn are similar to those in Embodiment 1. FIG. **5**B illustrates a cross-sectional view in this step.

Subsequently, without exposure of the oxide semiconductor film **103** containing In, Ga, and Zn to air, the gate insulating film **102** is deposited over the oxide semiconductor film **103** successively. When the gate insulating film **102** is deposited successively without exposure of the surface of the oxide semiconductor film **103** to air, productivity can be improved, and further, it is possible to form an interface between stacked layers where there is no contamination due to an atmospheric component such as moisture or an impurity element or a dust floating in air; therefore, variations in the characteristics of thin film transistors can be reduced.

In this specification, in successive deposition, a substrate to be processed is placed in an atmosphere which is controlled to be vacuum or an inert gas atmosphere (a nitrogen atmosphere or a rare gas atmosphere) at all times without being exposed

to a contaminant atmosphere such as air during a process from a first film formation step using a sputtering method to a second film formation step using a sputtering method. By the successive formation, a film can be formed while preventing moisture or the like from being attached again to the substrate to be processed which is cleaned.

For example, performing the process from the first film formation step to the second film formation step in the same chamber is within the scope of the successive formation in this specification.

In addition, the following is also within the scope of the successive formation in this specification: in the case of performing the process from the first film formation step to the second film formation step in plural chambers, the substrate is transferred after the first film formation step to another chamber without being exposed to air and subjected to the second film formation.

Note that between the first film formation step and the second film formation step, a substrate transfer step, an alignment step, a slow-cooling step, a step of heating or cooling the substrate to a temperature which is necessary for the second film formation step, or the like may be provided. Such a process is also within the scope of the successive formation in this specification.

A step in which liquid is used, such as a cleaning step, wet etching, or resist formation, may be provided between the first film formation step and the second film formation step. This case is not within the scope of the successive formation in this specification.

Note that here, following the deposition of the oxide semiconductor film **103**, as illustrated in FIG. **5**B, the gate insulating film **102** formed using a silicon oxide film is formed with the use of a multi-chamber sputtering apparatus provided with a silicon target and a target for the oxide semiconductor film.

Next, with the use of a resist mask **133** formed by a photolithography technique or an ink-jet method, the gate insulating film **102** and the oxide semiconductor film **103** containing In, Ga, and Zn are etched to form the oxide semiconductor layer **113** and the gate insulating layer **112** as illustrated in FIG. **5**C.

Next, a conductive film **101** which is to be a gate electrode layer is formed as illustrated in FIG. **5**D. The gate electrode layer can be formed in a manner similar to that of Embodiment 1. In this embodiment, a single layer of a high-melting-point metal conductive film is used.

Next, with the use of a resist mask **134** formed by a photolithography technique or an ink-jet method, the conductive film **101** is etched to form the gate electrode layer **111** as illustrated in FIG. **5**E.

By the method described above, the staggered thin film transistor illustrated in FIG. **4** is manufactured.

In the thin film transistor manufactured in this embodiment, with the surfaces of the source and drain electrode layers kept clean, the oxide semiconductor layer containing In, Ga, and Zn can be formed; therefore, contact resistance between the source and drain electrode layers and the oxide semiconductor layer containing In, Ga, and Zn can be reduced.

Accordingly, by applying the present invention, a thin film transistor having a high on/off ratio can be manufactured. Further, a semiconductor device which includes a thin film transistor having favorable electrical characteristics and reliability can be provided by a method which is excellent in productivity.

EXAMPLE 1

In this example, a case where a bottom gate thin film transistor is manufactured by the method for manufacturing a semiconductor device which is described in Embodiment 1 will be described. Further, electrical properties of the thin film transistor are compared to those of a thin film transistor which is manufactured without performing plasma treatment on surfaces of source and drain electrode layers.

In this example, plasma treatment was performed on the surfaces of the source and drain electrode layers by a reverse sputtering method. The conditions of a reverse sputtering method were as follows: RF sputtering was performed with a pressure in a chamber of 0.4 Pa, a flow rate of an Ar gas of 50 sccm, and a power of 200 W.

The thin film transistor manufactured has a gate insulating film formed using a silicon oxynitride film with a thickness of 100 nm over a gate electrode layer formed using a tungsten film with a thickness of 100 nm; source and drain electrode layers formed using a tungsten film with a thickness of 100 nm end portions of which overlap with the gate electrode layer with the gate insulating film interposed therebetween; and an oxide semiconductor layer formed using an IGZO film with a thickness of 50 nm over a channel formation region. The channel length and the channel width are 100 μm.

FIG. **6** shows the electrical properties (gate voltage-drain current characteristics, an I_d–V_g curve) of the thin film transistor in which after performing plasma treatment on the surfaces of the source and drain electrode layers by a reverse sputtering method, the oxide semiconductor layer containing In, Ga, and Zn is formed without exposure of the surfaces of the source and drain electrode layers to air.

As a comparative example, FIG. **7** shows an I_d–V_g curve of a thin film transistor in which the oxide semiconductor layer containing In, Ga, and Zn was formed without performing plasma treatment on the surfaces of the source and drain electrode layers. Note that the measurements were performed at a drain voltage (a voltage of a drain with respect to a voltage of a source) of 1 V and 10 V.

Comparing the I_d–V_g curve in FIG. **6** with that in FIG. **7**, it is found that the thin film transistor of FIG. **6** in which plasma treatment was performed on the surfaces of the source and drain electrode layers by a reverse sputtering method has higher ON current regardless of conditions of the drain voltages. Further, there is no large difference in off current.

By applying one embodiment of the present invention as described above, a thin film transistor which can obtain high ON current while suppressing off current, that is, a thin film transistor having a high on/off ratio can be manufactured. Further, one embodiment of the present invention provides a method for manufacturing a semiconductor device having favorable electrical properties and reliability with high productivity.

This application is based on Japanese Patent Application serial no. 2008-224061 filed with Japan Patent Office on Sep. 1, 2008, the entire contents of which are hereby incorporated by reference.

What is claimed is:

1. A method for manufacturing a semiconductor device, the method comprising the steps of:

forming an insulating film;

performing a plasma treatment on the insulating film;

after performing the plasma treatment, forming an oxide semiconductor film over the insulating film; and

performing a heat treatment on the oxide semiconductor film,

wherein the plasma treatment is performed in an atmosphere comprising oxygen, and

wherein the oxide semiconductor film comprises indium and zinc.

2. The method according to claim 1, comprising the step of:
forming a source electrode layer and a drain electrode layer over the insulating film,
wherein the plasma treatment is performed on the source electrode layer and the drain electrode layer, and
wherein the oxide semiconductor film is formed over the source electrode layer and the drain electrode layer.

3. The method according to claim 1, wherein the oxide semiconductor film is formed without exposure to air after the plasma treatment is performed.

4. The method according to claim 1, wherein the oxide semiconductor film comprises gallium.

5. The method according to claim 1, wherein the atmosphere comprises an inert gas.

6. The method according to claim 1, the method comprising the step of forming a gate electrode layer,
wherein the insulating film is formed over the gate electrode layer, and
wherein the oxide semiconductor film is formed to overlap the gate electrode layer.

7. The method according to claim 1, wherein the heat treatment is performed at a temperature higher than or equal to 200° C. and lower than or equal to 600° C.

8. The method according to claim 1, comprising the step of forming a gate electrode layer over the oxide semiconductor film.

9. A method for manufacturing a semiconductor device, the method comprising the steps of:
forming an insulating film;
performing a sputtering treatment on the insulating film;
after performing the sputtering treatment, forming an oxide semiconductor film over the insulating film; and
performing a heat treatment on the oxide semiconductor film,
wherein the sputtering treatment is performed in an atmosphere comprising oxygen, and
wherein the oxide semiconductor film comprises indium and zinc.

10. The method according to claim 9, comprising the step of:
forming a source electrode layer and a drain electrode layer over the insulating film,
wherein the sputtering treatment is performed on the source electrode layer and the drain electrode layer, and
wherein the oxide semiconductor film is formed over the source electrode layer and the drain electrode layer.

11. The method according to claim 9, wherein the oxide semiconductor film is formed without exposure to air after the sputtering treatment is performed.

12. The method according to claim 9, wherein the oxide semiconductor film comprises gallium.

13. The method according to claim 9, wherein the atmosphere comprises an inert gas.

14. The method according to claim 9, the method comprising the step of forming a gate electrode layer,
wherein the insulating film is formed over the gate electrode layer, and
wherein the oxide semiconductor film is formed to overlap the gate electrode layer.

15. The method according to claim 9, wherein the heat treatment is performed at a temperature higher than or equal to 200° C. and lower than or equal to 600° C.

16. The method according to claim 9, comprising the step of forming a gate electrode layer over the oxide semiconductor film.

17. A method for manufacturing a semiconductor device, the method comprising the steps of:
forming an insulating film;
performing a plasma treatment on the insulating film;
after performing the plasma treatment, forming an oxide semiconductor film over the insulating film; and
performing a heat treatment on the oxide semiconductor film,
wherein the plasma treatment is performed in an atmosphere comprising oxygen,
wherein the oxide semiconductor film comprises indium and zinc, and
wherein the oxide semiconductor film after performing the heat treatment has crystallinity and exhibits a peak in a range of $30° \leq 2\theta \leq 35°$ when the oxide semiconductor film is measured by an X-ray diffraction method.

18. The method according to claim 17, comprising the step of:
forming a source electrode layer and a drain electrode layer over the insulating film,
wherein the plasma treatment is performed on the source electrode layer and the drain electrode layer, and
wherein the oxide semiconductor film is formed over the source electrode layer and the drain electrode layer.

19. The method according to claim 17, wherein the oxide semiconductor film is formed without exposure to air after the plasma treatment is performed.

20. The method according to claim 17, wherein the oxide semiconductor film comprises gallium.

21. The method according to claim 17, wherein the atmosphere comprises an inert gas.

22. The method according to claim 17, the method comprising the step of forming a gate electrode layer,
wherein the insulating film is formed over the gate electrode layer, and
wherein the oxide semiconductor film is formed to overlap the gate electrode layer.

23. The method according to claim 17, wherein the heat treatment is performed at a temperature higher than or equal to 700° C.

24. The method according to claim 17, comprising the step of forming a gate electrode layer over the oxide semiconductor film.

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